AMENDMENTS TO THE CLAIMS

Kindly amend claims 1, 9-10, 13-14, and 21-23 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) An interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors, the interface comprising:

an instruction bus, configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, wherein particular instructions designate and direct one of the plurality of coprocessors to transfer the data to/from the CPU; and

a data bus, coupled to said instruction bus, configured to transfer the data, wherein data order signals within said data bus specify a data transfer order that differs from said instruction transfer order, and wherein said data order signals specify transfer of a data element, said data element corresponding to a specific outstanding instruction, wherein said data order is relative to outstanding instructions, said outstanding instructions being those of said particular instructions transferred to said one of the plurality of coprocessors that have not completed a data transfer;

wherein the interface keeps track of said data order, and wherein said data order signals indicate said data order, and wherein said data order signals are provided with said data element as said data element is transferred.

2. (Previously Presented) The interface as recited in claim 1 wherein the plurality of coprocessors comprises:

a first plurality of floating-point coprocessors; or

a first plurality of graphics (3-D) coprocessors; or

a second plurality of floating-point coprocessors and a second plurality of graphics (3-D) coprocessors.

3. (Previously Presented) The interface as recited in claim 1, wherein said particular instructions comprise TO instructions, said TO instructions directing that the transfer of the data will be from the CPU to said one of the plurality of coprocessors.

4. (Previously Presented) The interface as recited in claim 3, wherein said particular instructions comprise FROM instructions, said FROM instructions directing that the transfer of the data will be to the CPU from said one of the plurality of coprocessors.

5. (Previously Presented) The interface as recited in claim 4, wherein said data bus comprises:

data TO signals, for transferring data from the CPU to one of the plurality of coprocessors; and

data FROM signals, for transferring data to the CPU from said one of the plurality of coprocessors.

6. (Previously Presented) The interface as recited in claim 5, wherein said data order signals comprise:

TO order signals, for specifying said data transfer order with respect to transfers via said data TO signals; and

FROM order signals, for specifying said data transfer order with respect to transfers via said data FROM signals.

7. (Previously Presented) The interface as recited in claim 6, wherein said TO order signals prescribe a particular outstanding TO instruction that is relative in order to all outstanding TO instructions.

8. (Previously Presented) The interface as recited in claim 6, wherein said FROM order signals prescribe a particular outstanding FROM instruction that is relative in order to all outstanding FROM instructions.

9. (Currently Amended) The interface as recited in claim 1, wherein said data bus transfers the data ~~in parallel~~over parallel signal lines to said one of the plurality of coprocessors, wherein said one of the plurality of coprocessors has multiple issue pipelines providing for parallel instruction execution.

10. (Currently Amended) A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, wherein said computer readable program code, when used with the computing device, ~~for causing~~ causes enablement of functions corresponding to a coprocessor interface ~~to be described~~ that transfers data between CPU and a plurality of coprocessors, said computer readable program code comprising:

first program code, for ~~providing an~~causing enablement of functions corresponding to an instruction bus, said instruction bus configured to transfer instructions to said plurality of coprocessors in an instruction transfer order, wherein particular instructions designate and direct one of said plurality of coprocessors to transfer said data to/from said CPU; and

second program code, for ~~providing~~ acausing enablement of functions corresponding to a data bus, said data bus configured to transfer said data, wherein data order signals within said data bus specify a data transfer order that is different from said instruction transfer order, and wherein said data order signals specify transfer of a data element, said data element corresponding to a specific outstanding instruction, wherein said data order is relative to outstanding instructions, said outstanding instructions being those of said particular instructions transferred to said one of said plurality of coprocessors that have not completed a data transfer;

wherein the coprocessor interface keeps track of said data order, and wherein said data order signals indicate said data order, and wherein said data order signals are provided with said data element as said data element is transferred.

11. (Previously Presented) The computer program product as recited in claim 10, wherein said particular instructions comprise:

TO instructions, said TO instructions directing that the transfer of said data will be from said CPU to said one of said plurality of coprocessors; and

FROM instructions, said FROM instructions directing that the transfer of said data will be to said CPU from said one of said plurality of coprocessors.

12. (Previously Presented) The computer program product as recited in claim 11, wherein said data order signals comprise:

TO order signals, for specifying said data transfer order for a particular outstanding TO instruction that is relative in order to all outstanding TO instructions; and

FROM order signals, for specifying said data transfer order for a particular outstanding FROM instruction that is relative in order to all outstanding FROM instructions.

13. (Currently Amended) The computer program product as recited in claim 10, wherein said data bus is configured to transfer said data over parallel signal lines~~in parallel~~ to particular coprocessors that have multiple issue pipelines providing for parallel instruction execution and corresponding data transfers.

14. (Currently Amended) An apparatus for transmitting program code, comprising:

a communication network having a transmission medium, for embodying a computer data signal therein, the computer data signal comprising:

computer-readable first program code, for use with a computing device, wherein said computer-readable first program code, when used with said computing device, causes enablement of functions corresponding to ~~for providing~~ an instruction bus for transferring instructions to a plurality of coprocessors in an instruction transfer order, wherein particular instructions designate and direct a particular coprocessor to transfer data to/from a CPU; and

computer-readable second program code, for use with said computing device, wherein said computer-readable second program code, when used with said computing device, causes enablement of functions corresponding to~~for providing~~ a data bus for transferring said data, wherein data order signals within said data bus specify a data transfer order that differs from said instruction transfer order, and wherein said data order signals specify transfer of a data element, said data element corresponding to a specific outstanding instruction, wherein said data order is relative to outstanding instructions, said outstanding instructions being those of said particular instructions transferred to said particular coprocessor that have not completed a data transfer;

wherein said data order signals indicate said data order, and wherein said data order signals are provided with said data element as said data element is transferred.

15. (Previously Presented) The apparatus as recited in claim 14, wherein said particular instructions comprise TO instructions, said TO instructions directing that transfer of said data will be from said CPU to said particular coprocessors.

16. (Previously Presented) The computer data signal as recited in claim 15, wherein said particular instructions comprise FROM instructions, said FROM instructions directing that the transfer of said data will be to said CPU from said particular coprocessors.

17. (Previously Presented) The apparatus as recited in claim 14, wherein said data bus comprises:

data TO signals, for transferring data from said CPU to said particular coprocessor; and

data FROM signals, for transferring data to said CPU from said particular coprocessor.

18. (Previously Presented) The apparatus as recited in claim 17, wherein said data order signals comprise:

TO order signals, for specifying said data transfer order with respect to transfers via said data TO signals; and

FROM order signals, for specifying said data transfer order with respect to transfers via said data FROM signals.

19. (Previously Presented) The apparatus as recited in claim 18, wherein said TO order signals specify a particular outstanding TO instruction that is relative in order to all outstanding TO instructions.

20. (Previously Presented) The apparatus as recited in claim 18, wherein said FROM order signals specify a particular outstanding FROM instruction that is relative in order to all outstanding FROM instructions.

21. (Currently Amended) The apparatus as recited in claim 14, wherein said data bus transfers said data over parallel signal lines~~in parallel~~ to selected coprocessors, said selected coprocessors having multiple issue execution pipelines.

22. (Currently Amended) A method for transferring data between a CPU and a plurality of coprocessors, the method comprising:

transmitting instructions to one of the plurality of coprocessors, each of the instructions designating the one of the plurality of coprocessors, and each of the instructions directing a data transfer between the CPU and the one of the plurality of coprocessors, wherein said transmitting is provided in a specific instruction order; and

transferring the data in an order different from the specific instruction order, said transferring comprising:

specifying transfer of a data element corresponding to a specific outstanding instruction, wherein the order of said transferring is relative to outstanding instructions, the outstanding instructions being those of the instructions transmitted to the one of the plurality of coprocessors that have not completed a data transfer; and

providing the data order signals with the data element as the data element is transferred.

23. (Currently Amended) The method as recited in claim 22, said transmitting comprises:

issuing a plurality of the instructions ~~in parallel~~over parallel signal lines to the one of the plurality of coprocessors; and

designating an execution order ~~corresponding to said issuing~~for the plurality of the instructions.